27.5 High-Speed Digital Double Sampling with Analog CDS on Column Parallel ADC Architecture for Low-Noise Active Pixel Sensor

Yoshikazu Nitta, Yoshinori Muramatsu, Kiyotaka Amano, Takayuki Toyama, JunYamamoto, Koji Mishina, Atsushi Suzuki, Tadayuki Taura, Akihiko Kato, Masaru Kikuchi, Yukihiro Yasui, Hideo Nomura, Noriyuki Fukushima

Sony, Atsugi, Japan

Traditionally, the advantages of compact image sensors (CISs) over CCDs have been low power consumption and the capability for system integration. Additionally, the image quality of CISs has recently begun to rival and even surpass that of CCDs in the area of high-speed imaging [1]. Compared to high-speed CCDs, CISs utilize the advantage of a column-parallel pixel readout. Column-parallel ADCs allow for low-bandwidth readouts. This is a key advantage over wide-bandwidth single-output amplifiers in CCDs or single ADC CISs. In order to realize these high-speeds, CISs need to simultaneously achieve a high-speed data rate and high image quality (equivalent to that of CCDs). A progressive 1/1.8-inch 1920×1440 CMOS image sensor with a column-inline dual-CDS architecture is designed in a 0.18μm CMOS process. This architecture implements high-speed digital sampling with analog CDS on column-parallel ADC for high-speed and high-quality imaging. Random noise is $5.2e^-_{rms}$ at 180frames/s. The dynamic range at 180frames/s (corresponding to a 600MHz rate and 6.0Gb/s) is 68dB. The FPN is $<0.5e^-_{rms}$ without the additional FPN-correction circuit.

This CIS is composed of 6 main parts. 1) a 1920×1440 pixel array, 2) 1440 row decoders and drivers, 3) 1920 column parallel ADCs, 4) a single-slope ramp generator DAC with 12b accuracy, 5) digital logic control, and 6) a 12b LVDS interface (at a frequency of up to 600MHz). Figure 27.5.1 shows the block diagram of the whole system. The CIS operates with a single master clock at 74.25MHz. Additionally, a PLL generates a 297MHz clock, ϕ_{PLL}, quadruple the master clock. This clock is supplied to the column ADCs, slope DAC, and the LVDS interface.

The pixels are conventional 4T active pixel sensor (APS) pixels that use hole accumulation diodes (HADs). HADs enable image sensors such as CCDs and CISs to realize ideal properties of low dark current, no kTC noise, and no image lag [2]. Pixel operation requires 3 control signals, ϕ_S, ϕ_T, and ϕ_R controlled by row decoders.

Digital double-sampling architecture is proposed to remove device variation and circuit offset that cause vertical FPN [3]. Our column-inline dual-CDS architecture (Fig. 27.5.2) implements digital double-sampling (digital CDS) and analog CDS in parallel columns. A high-speed 297MHz clock is utilized to reduce the double digital sampling period. Additionally, an analog CDS is used to reduce the ADC period for the reset signal V_{RST} by eliminating the analog offset of the pixel and the comparator output.

The column-parallel ADCs are composed of parallel banks of comparators and counters. The column comparators are driven by a ramp generator DAC and the pixel output by connecting series capacitor C_1. The column counters, composed of ripple counters, perform the A/D conversion by counting the number of clocks (ϕ_{PLL}) until the comparator output changes. Ripple counters have the advantage of not needing to be synchronized with the high-speed clock ϕ_{PLL}. Digital CDS is obtained by changing up/down counting of the ripple counters using the clock selectors. Column-to-column variations of clock skew and counter delay that cause A/D conversion error are corrected by digital CDS.

Figure 27.5.3 shows the readout timing chart for the column-inline dual-CDS architecture. The sequence is as follows: 1) the reset control signal ϕ_R resets the pixels causing the reset level of the sensor output to appear at the vertical pixel output. 2) The input and output of the comparators are connected through transistor S1. This eliminates the offset of the comparators and the pixel outputs that causes FPN when the control signal ϕ_{AZ} is turned on (analog CDS stage). 3) The A/D conversion of the reset signal is performed by counting the number of digital clock ϕ_{PLL} cycles until the analog ramp voltage matches the vertical pixel output voltage. The ripple counters are set to down counting period by the signal ϕ_{UD}. 4) The signal level appears at the sensor output when the control signal ϕ_T opens the transfer gate. 5) The counters, which are set to up counting period, digitally subtract the conversion of the reset signal from the sensor signal after the charge transfer from the photodiode (digital CDS stage). By using dual CDS, the analog pixel signal is converted to the corrected digital output signal in the individual columns in parallel. When the dual CDS is finished, the digital data is transferred to the column latches included in each counter block. This pipelines the A/D conversion and horizontal data transfer.

Using high-speed clock and analog CDS, the 12b ADC achieves a data rate of 150MHz. However, the resolution of dual-ADC architecture is restricted by the number of clock cycles in the conversion time. In other words, the increased frame rate limits the time for the A/D conversion. According to the length of the conversion time, the resolution of the analog slope DAC is variable from 10b to 12b. In the case of 180frames/s with a maximum data rate of 600MHz, the resolution of the ADC is 10b. Maximum clock speed is limited by the power consumption and comparator slew rate.

Figure 27.5.4 shows a chip micrograph of the fabricated CMOS image sensor. The size of the imaging region is 7.0mm(H)×5.2mm(V) compatible with the 1/1.8-inch optical format. A 0.18μm 1P3M CMOS sensor process is employed for fabrication. A sample image taken with the sensor at 180frames/s is shown in Fig. 27.5.5. Image distortion due to the rolling shutter is negligible at 180frames/s. The Image quality of high speed is maintained with this architecture.

Chip characteristics are summarized in Fig. 27.5.6. The measurements are performed with the sensor running at 60frames/s and with an ADC reference voltage of 1V in 12b accuracy. The measured readout random noise is $4.8e^-_{rms}$. The random noise at maximum frame rate of 180frames/s is $5.2e^-_{rms}$, which is slightly worse compared with 60frames/s because of the increasing noise on the voltage supplies. The dark vertical FPN is $0.5e^-_{rms}$ without the additional FPN-correction circuit. The dynamic range is 68dB and the data rate delivered by the sensor at the maximum frame rate approaches 6Gb/s.

References:

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[3] W. Yang, O. Kwon, J. Lee, G. Hwang, S. Lee, "Integrated 800×600 CMOS Imaging System," *ISSCC Dig. Tech. Papers*, pp.304-305, Feb., 1999.

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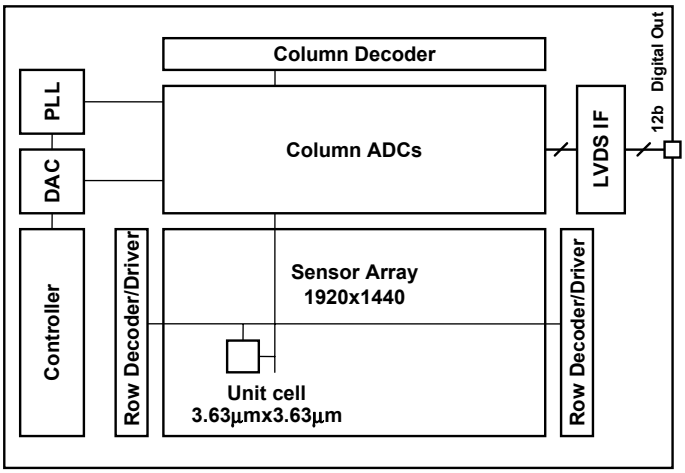

Figure 27.5.1: Block diagram.

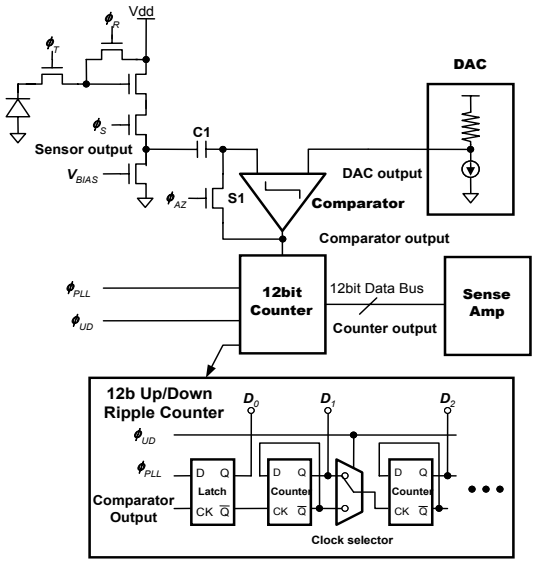

Figure 27.5.2: Column-inline dual CDS architecture.

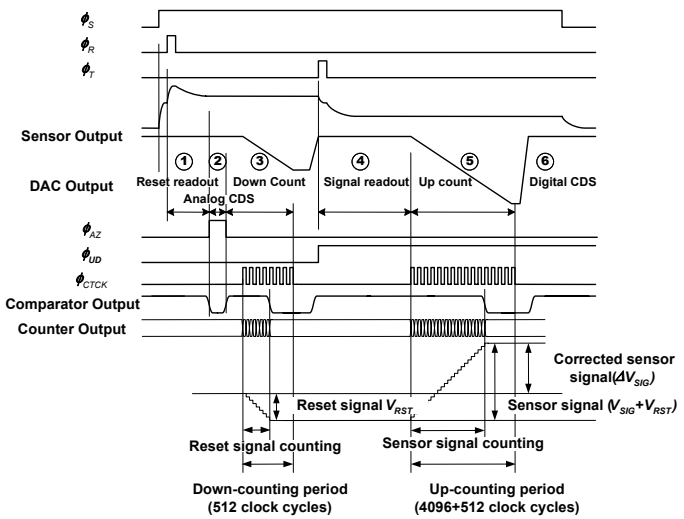

Figure 27.5.3: Timing diagram.

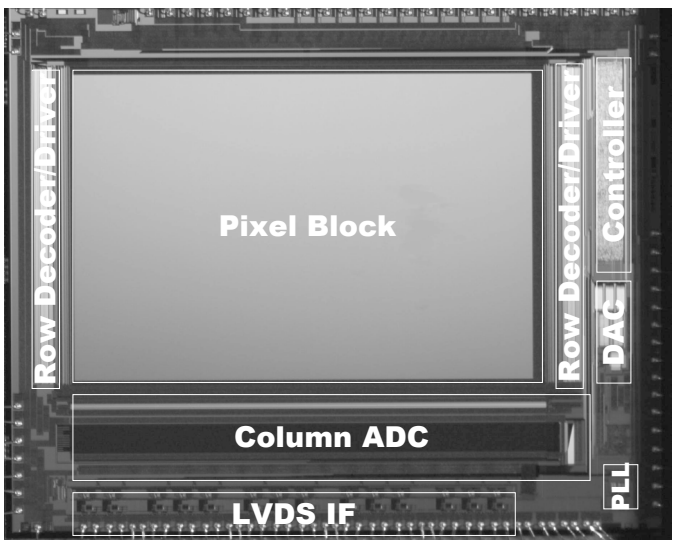

Figure 27.5.4: Chip micrograph.

Figure 27.5.5: Sample images.

Process	0.18µm 1P 3M
Supply Voltage	3.3V / 1.8V
Number of effective pixels	1920 (H) x 1440 (V)
Pixel size	3.63 µm (H) x 3.63 µm (V)
Aperture ratio	41% without on-chip microlens
Max. data rate	600MHz (300MHz DDR)
Max. frame rate	180frames/s
Power consumption	580mW at 180frames/s
Saturation signal	15,000e^- at 60 C
Sensitivity	30,000e^-/lx-s At 3200k light source with IR cut filter of 650nm cut-off
Image lag	Below measurement threshold
Dark current	15.9e^-/s at 60 C
rms random noise	4.8e^-_{rms} at 60fps, 5.2e^-_{rms} at 180frames/s
rms vertical FPN	0.5e^-_{rms} at 60fps w/o additional correction circuit
Dynamic range	68dB at 180frames/s
Conversion gain	63µV/e^-

Figure 27.5.6: Chip characteristics.

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